1. Briefly distinguish between full-custom ASICs, standard-cell-based ASICs, and FPLDs, in terms of fabrication, design techniques employed, layout of components, etc. (25 points)
2. In studying combinational circuit design, we concentrated on the Sum-of-Products (SOP) form of Boolean expressions.

a. Why is SOP form useful and/or of particular interest? (10 points)

b. Considering the relationship between a Karnaugh map and an equivalent SOP expression, why is it desirable to make the ovals as large as possible? Be specific. (10 points)

3. Before programming a design into a FPLD, it is generally considered a good idea to verify the design’s functionality using the simulator.

a. Why is simulating the design important, given it only takes a few seconds to download the design onto the FPLD where you can test the “real” design? (10 points)
b. In the tutorial example with the two pushbuttons and the OR gate, why was the one pushbutton simulated with the default clock frequency, while the other was simulated with a clock frequency double the default value? (10 points)

4. The diagram below shows how a D latch can be constructed from an SR latch.

![Diagram of SR latch and D latch]

a. What “problem” does an SR latch have, that prompts the development of a D latch? (10 points)

b. What is the difference between this D latch and a D flip-flop? (10 points)
5. There are many different types of FPLDs. This question explores those differences.
   a. Between antifuse-based and SRAM-based FPLDs, which allows more chip space to be dedicated to combinational / sequential logic, and why? (10 points)
   b. Why is it desirable to find some way to “segment” a particular track in a routing channel into two or more segments? (5 points)