Types of ASICs

- IC contains a chip (“die”) cut from a wafer
  - Transistors, wires, etc. are built up on the chip in a series of layers (10-15 layers)
  - A mask is used to define the components of a layer as they are applied to the chip

Types of ASICs (and pizza equivalent)

- Full-custom ASIC
  - Pizza built from scratch, takes a long time to prepare and cook
- Standard-cell-based ASIC
  - Custom-built from predefined selection, takes a long time to cook
- Gate-array-based ASIC
  - Pre-cooked crusts, predefined selections, cooks quickly, somewhat cheaper
- Field-programmable logic device
  - Frozen pizza — limited selection, cook it yourself at home, very cheap

Full-Custom ASICs

- Engineer designs some or all of the logic cells, circuit, and layout
- Mostly used:
  - If no pre-designed cells are available (e.g., new or highly specialized circuit)
  - If high-performance, less area, lower power, etc. is needed
- Fabricated in batches of 5 to 30 wafer lots, each wafer containing 10–100 chips
- Various technologies used (details later):
  - Bipolar — legacy from analog circuits, more consistent characteristics of components across chip / wafer
  - CMOS — more widely available, lots of cells and tools, wave of the future (at least for now)

Standard-Cell-Based ASICs

- Chip is built from pre-defined logic cells (gates, adders, etc.) called standard cells
  - Standard cells are built by someone else using full-custom design techniques
  - Save time, money, and risk by using a predesigned, pretested cell library
    - But — have to pay for the cell library
  - Also use larger cells (microprocessors, etc.) called mega cells (sometimes cores)

- Cells fit together like bricks in a wall — rows of (variable-width) cells
  - Most interconnect goes in channels between rows
  - Some cells may be designated as feedthroughs between rows
  - Other metal layers also provide interconnect
    - Connection between layers is called a via

Figure from Application-Specific Integrated Circuits, Smith, Addison-Wesley, 1997
### Gate-Array-Based ASICs

- Transistors are predefined in a fixed pattern on the chip
  - Interconnect is defined by designer and fabricated using a custom mask
  - Designer chooses cells from a gate-array library of predefined, pretested cells

- Chip is partially fabricated (cells, power, etc. added) and then stockpiled
  - When design is received for fabrication, the remaining metal layers are added
  - Cheaper — everyone shares cost of producing high volume of initial chip
  - Quick turn-around — days, couple weeks

**Variations:**
- Channeled gate arrays
- Channelless gate arrays

### Programmable Logic Devices (PLDs)

- Standard ICs, available in standard configurations, sold in high volume
  - But can be configured / programmed to create a specialized device
  - No customized cells or masks, just a single large block of programmable interconnect
  - Fast turn-around time

**Examples**
- Mask-programmable ROM — programmed when ordered
- Programmable ROM — programmed electrically, erased electrically or using ultraviolet light, all by customer
- PAL, PLA — 2-level sum-of-products and/or array, programmed electrically by customer (blowing fuses in array)

### Field Programmable Logic Devices (FPLDs)

- Known by a variety of names:
  - Field-Programmable Gate Array (FPGA)
  - Field-Programmable Logic Device (FPLD)
  - Complex Programmable Logic Device (CPLD)

- Similar to PLDs, but more complex
  - No customized mask layers
  - Some method for programming the base logic cells and the interconnect
  - Core is a regular array of programmable logic cells, each of which contains combinational and sequential logic
  - Programmable interconnect surrounds the logic cells
  - Design turn-around is on the order of hours

### Economics of ASICs

- For a given design, which type of ASIC is the most cost-effective?
  - (full-custom) ASIC?
  - MGA (mask-programmable gate array)?
  - CBIC (cell-based integrated circuit = standard-cell-based ASIC)?

**Answer:** consider the ASIC as a product, and examine the fixed costs and variable costs

- total product cost = fixed product cost + variable product cost
- **Fixed product cost** is independent of sales volume
  - Fixed product costs amortized per product sold decrease as sales volume increases
- **Variable product cost** includes assembly costs and manufacturing costs
Example of ASIC Economics

- Sample costs:
  - CBIC: fixed cost $146,000; part cost $8
  - MGA: fixed cost $86,000; part cost $10
  - FPGA: fixed cost $21,800; part cost $39

Break-even points:
- FPGA to MGA is around 2,000 parts
- FPGA to CBIC is around 4,000 parts
- MGA to CBIC is around 20,000 parts

Figure from Application-Specific Integrated Circuits, Smith, Addison-Wesley, 1997

ASIC Fixed Costs

- Design: estimate of designer productivity
- Production test: make sure the IC works
- Non-recurring engineering (NRE): work done by ASIC vendor — developing mask, production tests, prototypes, etc.

<table>
<thead>
<tr>
<th></th>
<th>FPGA</th>
<th>MGA</th>
<th>O/B</th>
</tr>
</thead>
<tbody>
<tr>
<td>Training</td>
<td>$600</td>
<td>$600</td>
<td>$600</td>
</tr>
<tr>
<td>NRE</td>
<td>$400</td>
<td>$400</td>
<td>$400</td>
</tr>
<tr>
<td>Design</td>
<td>$80,000</td>
<td>$80,000</td>
<td>$80,000</td>
</tr>
<tr>
<td>Fabrication</td>
<td>200,000</td>
<td>200,000</td>
<td>200,000</td>
</tr>
<tr>
<td>Days</td>
<td>50</td>
<td>50</td>
<td>50</td>
</tr>
<tr>
<td>Cost/Part</td>
<td>$400</td>
<td>$400</td>
<td>$400</td>
</tr>
<tr>
<td>Design for test</td>
<td>$600</td>
<td>$600</td>
<td>$600</td>
</tr>
<tr>
<td>NRE</td>
<td>$80,000</td>
<td>$80,000</td>
<td>$80,000</td>
</tr>
<tr>
<td>Total fixed costs</td>
<td>$81,000</td>
<td>$80,000</td>
<td>$161,000</td>
</tr>
</tbody>
</table>

Figure from Application-Specific Integrated Circuits, Smith, Addison-Wesley, 1997

ASIC Variable Costs

- Wafer size: 6" & 8" common, 12" soon
- 10k gates = small design, 100k = large
- Gate utilization: space used for gates, not used for interconnect
- Defect density is measure of fabrication quality (defect on a die is usually fatal)
- Yield is percentage of usable dies

<table>
<thead>
<tr>
<th></th>
<th>FPGA (400)</th>
<th>MGA (200)</th>
<th>CBIC (50)</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Wafers</td>
<td>6</td>
<td>6</td>
<td>6</td>
<td>6</td>
</tr>
<tr>
<td>Wafer cost</td>
<td>$400</td>
<td>$1,000</td>
<td>$1,000</td>
<td>6</td>
</tr>
<tr>
<td>Design</td>
<td>$10,000</td>
<td>$10,000</td>
<td>$10,000</td>
<td>gates</td>
</tr>
<tr>
<td>Density</td>
<td>100k gates</td>
<td>200k gates</td>
<td>250k gates</td>
<td>gates/cm²</td>
</tr>
<tr>
<td>Utilization</td>
<td>65</td>
<td>65</td>
<td>65</td>
<td>%</td>
</tr>
<tr>
<td>Defect rate</td>
<td>$0.005</td>
<td>0.005</td>
<td>0.005</td>
<td>defect/cm²</td>
</tr>
<tr>
<td>Defects</td>
<td>100</td>
<td>200</td>
<td>50</td>
<td>parts</td>
</tr>
<tr>
<td>Yield</td>
<td>65%</td>
<td>75%</td>
<td>90%</td>
<td>%</td>
</tr>
<tr>
<td>Proficiency</td>
<td>90%</td>
<td>90%</td>
<td>90%</td>
<td>%</td>
</tr>
<tr>
<td>Product</td>
<td>90</td>
<td>90</td>
<td>90</td>
<td>parts</td>
</tr>
<tr>
<td>Part cost</td>
<td>$30</td>
<td>$100</td>
<td>$90</td>
<td></td>
</tr>
</tbody>
</table>

Figure from Application-Specific Integrated Circuits, Smith, Addison-Wesley, 1997