# Types of FPLDs

## Type of Base Cell

<table>
<thead>
<tr>
<th>Multiplexer</th>
<th>Look-Up Table (LUT)</th>
<th>AND-OR</th>
</tr>
</thead>
<tbody>
<tr>
<td>Antifuse</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Actel</td>
<td>ACT 1, ACT 2, ACT 3</td>
<td></td>
</tr>
<tr>
<td>Quicklogic</td>
<td>Crosspoint</td>
<td></td>
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<tr>
<td>EPROM</td>
<td></td>
<td></td>
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<tr>
<td>Altera MAX</td>
<td>5000, 7000</td>
<td></td>
</tr>
<tr>
<td>(Salcic 2.1)</td>
<td></td>
<td></td>
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<tr>
<td>Xilinx</td>
<td>EPLD</td>
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<tr>
<td>SRAM</td>
<td>Plessy</td>
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<tr>
<td>Altera Flex</td>
<td>8000, Flex 10K</td>
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<tr>
<td>(Salcic 2.2)</td>
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<tr>
<td>Xilinx LCA</td>
<td>2000, 3000, 4000</td>
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<tr>
<td>(Salcic 2.3)</td>
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</tbody>
</table>

## Programming Method

- **Antifuse**
- **EPROM**
- **SRAM**

## FPGAs

- **Row-Based Layout**

  - Cells are arranged in rows
  - Horizontal channels between rows
  - Vertical channels above cells: some short, some long
  - Each channel contains a fixed number of tracks, each track holds one wire
    - Wires may be divided into fixed-length segments within each track
  - In figure above, cell inputs connect to horizontal wires, outputs to vertical wires

## CPLDs

- **Matrix-Based Layout**

  - Cells are arranged in an array (matrix)
  - Horizontal and vertical channels between cells
  - Each channel contains a fixed number of tracks, each track holds one wire
  - In figure above:
    - Cell inputs connect to horizontal tracks
    - Box A connects cell output(s) to horizontal tracks, and box C connects cell output(s) to vertical tracks
    - Box B acts as a switchbox between horizontal and vertical tracks

## Antifuse Routing

- **Antifuse Routing**

  - (a) routing in unconstrained channel
  - (b) routing in fully segmented channel
  - (c) routing in non-segmented channel
  - (d) segmented for 1-segment routing
  - (e) segmented for 2-segment routing

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*Figures from Application-Specific Integrated Circuits, Smith, Addison-Wesley, 1997 and Field-Programmable Gate Array Technology, Trimberger, Kluwer, 1994*
Antifuse Routing (cont.)

- **Fully segmented**
  - Switch at every cross point normally passes signals through vertically and horizontally, but can connect the vertical and horizontal tracks
  - Antifuse connects or disconnects the segments of the horizontal channel

- **Non-segmented**
  - Excessive area requirements

- **1-segment routing**
  - Divides the tracks into segments of varying lengths, which allows each net to be routed in a track of more or less the appropriate size

- **2-segment routing**
  - Allows track segments to be joined

Actel ACT Routing Architecture

- An Actel FPGA has rows of cells, with horizontal channels between them, and vertical “channels” called columns

- Cell inputs must come from one of the 2 adjacent horizontal tracks (either figure)

- Cell outputs can attach to:
  - A dedicated vertical track called the “output stub” (see bottom figure)
    - Output stub spans only two channels above and below the cell
  - Long vertical tracks— see top figure, where output goes to LVT instead of its dedicated output segment
    - These are vertical segments of varying lengths that can be joined together to form vertical segmented tracks

- Input segments connect to uncommitted horizontal segment by antifuses
  - Horizontal segments connect by antifuses

- Vertical segments pass over the cells
Fairly simple, fine-grained logic module

- Low delay, small area, very flexible
- Implements basic gates, D latches, etc.
  - Can implement many functions using Shannon's Expansion Theorem
    - Any combinatorial function of 2 inputs
    - Almost any function of 3 inputs, many functions of 4 inputs, some functions of up to 8 inputs

I/O modules at end of rows & columns

C-module = combinatorial module

- Act2 c-module provides high fan-in
  - Can implement 16 of the 20 four-input gates in the library (Act1 implements 8)
  - Implements 766 distinct combinational functions, including 13% more four-input macros and 12% more five-input macros than Act1
  - Some loss in ability to implement sequential functions

S-module = sequential module

- C-module plus two latches
  - Can provide rising- or falling-edge-triggered D flip-flop, or high- or low-level transparent D latch, with clear
  - Can make it look like a c-module by tying C1 to 1 and C2 to 0
  - Need two or more s-modules to build J-K or more complex flip-flops

Note that the timing of a particular logic macro may vary with its implementation